1. A method for compressing a sequence of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for an element of a processor, the method comprising:

identifying a set of aligned fields that contain NOP instructions in each control words of the sequence of multiple-instruction control words;

modifying the sequence of multiple-instruction control words to remove the set of aligned fields;

storing an identifier that identifies the set of aligned fields removed; and

storing the modified sequence of multiple-instruction control words.

2. A method in accordance with claim 1, wherein the sequence of multiple-instruction control words is an inner loop of a computation.

3. A method in accordance with claim 1, wherein the sequence of multiple-instruction control words is a dataflow graph for a streaming vector processor.

4. A method in accordance with claim 1, wherein a control word of the sequence of multiple-instruction control words is a VLIW.

5. A method in accordance with claim 1, wherein the identifier is a compression mask having one bit associated with each field of the multiple-instruction control word.

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6. A method for processing a compressed sequence of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for an element of a processor, the method comprising:

fetching an identifier that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words;

for each control word of the compressed sequence of multiple-instruction control words;

fetching a control word;

reconstructing a corresponding uncompressed control word by inserting NOP instructions into the compressed control word in accordance with the identifier; and

providing the decompressed control word to the processor for execution.

7. A method in accordance with claim 6, wherein the processor further comprises a plurality of memory banks, the method further comprising:

enabling a subset of the plurality of memory banks sufficient to store one or more control words of the compressed sequence of multiple-instruction control words in accordance with the identifier;

disabling other memory banks of the plurality of memory banks; and

for each control word of the compressed sequence of control words:

storing the control word in the enabled subset of memory banks.

8. A method in accordance with claim 6, further comprising disabling unused elements of the processor in accordance with the identifier.

9. A method in accordance with claim 6, wherein the identifier is a compression mask having one bit associated with each field of the multiple-instruction control word.

10. A system for processing a compressed sequence of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for an element of a processor, the system comprising:

a mask latch for storing a compression mask that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words;

a logic unit coupled to the mask latch and responsive to the compression mask;

a memory for storing one or more compressed multiple-instruction control words;

a pipelined permute unit, coupled to the logic unit and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask; and

an instruction register, coupled the pipelined permute unit and operable to present reconstructed multiple-instruction control words to the processor.

11. A system in accordance with claim 10, wherein the memory comprises a plurality

of memory banks coupled to the logic unit, and wherein the logic unit is operable to disable memory banks in accordance with the compression mask.

12. A system in accordance with claim 10, further comprising:

a plurality of processing elements coupled to the mask latch and the instruction register and controlled by the reconstructed multiple-instruction control words,

wherein the compression mask is used to disabled processing elements of the plurality of processing elements that are unused by the sequence of multiple-instruction control words.

13. A system in accordance with claim 12, wherein the plurality of processing elements form part of a re-configurable streaming vector processor, and wherein the sequence of multiple-instruction control words is a sequence of VLIWs describing a dataflow graph.